```
**********************************************************
    5444 Thu Feb 12 20:33:30 2015
new/usr/src/uts/armv6/ml/cache.s
armv6: p15 cache functions say that value passed in should be zero
**********************************************************
______unchanged_portion_omitted_

 191         ENTRY(armv6_icache_inval)
 192         mov     r0, #0
 193 #endif /* ! codereview */
 194         mcr     p15, 0, r0, c7, c5, 0           @ Invalidate i-cache
 195         bx      lr
 196         SET_SIZE(armv6_icache_inval)

 198         ENTRY(armv6_dcache_inval)
 199         mov     r0, #0
 200 #endif /* ! codereview */
 201         mcr     p15, 0, r0, c7, c6, 0           @ Invalidate d-cache
 202         ARM_DSB_INSTR(r2)
 203         bx      lr
 204         SET_SIZE(armv6_dcache_inval)

 206         ENTRY(armv6_dcache_flush)
 207         mov     r0, #0
 208 #endif /* ! codereview */
 209         mcr     p15, 0, r0, c7, c10, 4          @ Flush d-cache
 210         ARM_DSB_INSTR(r2)
 211         bx      lr
 212         SET_SIZE(armv6_dcache_flush)
 213
 214         ENTRY(armv6_text_flush_range)
 215         add     r1, r1, r0
 216         sub     r1, r1, r0
 217         mcrr    p15, 0, r1, r0, c5              @ Invalidate i-cache range
 218         mcrr    p15, 0, r1, r0, c12             @ Flush d-cache range
 219         ARM_DSB_INSTR(r2)
 220         ARM_ISB_INSTR(r2)
 221         bx      lr
 222         SET_SIZE(armv6_text_flush_range)

 224         ENTRY(armv6_text_flush)
 225         mov     r0, #0
 226 #endif /* ! codereview */
 227         mcr     p15, 0, r0, c7, c5, 0           @ Invalidate i-cache
 228         mcr     p15, 0, r0, c7, c10, 4          @ Flush d-cache
 229         ARM_DSB_INSTR(r2)
 230         ARM_ISB_INSTR(r2)
 231         bx      lr
 232         SET_SIZE(armv6_text_flush)

 234 #endif

 236 #ifdef __lint

 238 /*
 239  * Perform all of the operations necessary for tlb maintenance after an update
 240  * to the page tables.
 241  */
 242 void
 243 armv6_tlb_sync(void)
 244 {}

 246 #else   /* __lint */

 248         ENTRY(armv6_tlb_sync)
 249         mov     r0, #0
```



```
 250         mcr     p15, 0, r0, c7, c10, 4          @ Flush d-cache
 251         ARM_DSB_INSTR(r0)
 252         mcr     p15, 0, r0, c8, c7, 0           @ invalidate tlb
 253         mcr     p15, 0, r0, c8, c5, 0           @ Invalidate I-cache + btc
 254         ARM_DSB_INSTR(r0)
 255         ARM_ISB_INSTR(r0)
 256         bx      lr
 257         SET_SIZE(armv6_tlb_sync)

 259 #endif  /* __lint */
```